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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,258	08/01/2003	David Dice	SUN03-09(030125)	4788

7590 10/06/2006

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EXAMINER	
BATAILLE, PIERRE MICHE	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 10/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,258	DICE, DAVID	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-23,43-46,48 and 49* is/are allowed.

6)☒ Claim(s) *1,2,6,24,25,29 and 47* is/are rejected.

7)☒ Claim(s) *3-5,7-19,26-28 and 30-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office action is taken in conjunction to examination of Application No. 10/633,258 filed 01 August 2003 presenting claims 1-49 for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-2, 6, 24-25, 29, and 47 rejected under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior art.

With respect to claims 1, 24 and 47, Applicant's Admitted Prior Art (AAPA) discloses a method for identifying processes to be executed a multiprocessing computer system having a plurality of processing devices, comprising:

detecting when a first process executing on a first processing device releases access to shared data;

in response to the first process releasing access to the shared data, attempting to identify a second process that:

i) formerly executed on the first processing device; and

ii) is awaiting access to the shared data; and

providing, to a kernel responsible for selecting processes to execute amongst the plurality of processing devices, an identification of the second process as a process that is ready for execution in the multiprocessing computer system.

AAPA discloses, correspondingly, a conventional kernel that uses affinity-based scheduling in a multiprocessing computer system, the kernel thus attempts to restart a pre-empted thread on a processing device that is associated with the same cache that stored the execution state information for that thread during its former execution (i.e. restarting a pre-empted thread meaning a process or thread that has been blocked during execution and is awaiting a chance for re-execution; in this case a block process automatically enters a queue of awaited processes awaiting execution).

Page 2 (lines 15-30) explicitly discusses the execution time slot for a thread to execute on a processing device. "When the time slot or an executing thread has expired, or if some other event such as an interrupt or a change in thread priority occurs, the kernel can remove or preempt the executing thread from execution on the processing device and can select and resume execution of another thread on that processing device. The kernel can perform this repetitive scheduling process involving thread selection and execution in a continuous manner for all processing devices in the multiprocessing computer system so that when a thread on one processing device is blocked from execution for some

reason (e.g., because its timeslot ended, or it become blocked awaiting access to shared memory or an input-output device or for some other reason), the kernel can select another thread for execution on that processing device."

Page 2 (lines 10-14 explains that the processing device has knowledge of the values for variables and/or other execution state information associated with the thread (i.e. identification o the thread) for faster access when this information is needed during execution of that thread as the processing device executes the thread of instructions of a software program (see page 2, Lines 22-30; page 4, lines 22-26).

Therefore,

(1) each thread of instructions that is awaiting its chance to execute is scheduled by the kernel to execute on a processing device;

(2) the kernel, providing execution timing for each thread monitors when the time slot or an executing time slot for a thread has expired;

(3) the kernel performs repetitive schedule and selection process and attempts to restart a thread that has been blocked and is awaiting an access on the shared device.

With respect to claims 2 and 25, AAPA discloses conventional affinity-based thread scheduling a thread that executes on the same processing device as was used for prior execution such that each thread of instructions that is awaiting its chance to execute is scheduled by the kernel to execute on the same processing device and the kernel

performs attempts to restart a thread that has been blocked and is awaiting a access on the shared device [Page 4, Lines 22-26].

With respect to claims 6 and 29, The method of claim 1 wherein attempting to identify a second process that formerly executed on the first processing device and that is awaiting to access shared data comprises: reviewing execution state associated with respective blocked processes awaiting access to the shared data; and if the execution state of a blocked process indicates that the blocked process formerly executed on the first processing device, identifying that blocked process as the second process [reviewing execution state associated with respective blocked processes awaiting access to the shared data; and if the execution state of a blocked process indicates that the blocked process formerly executed on the first processing device, identifying that blocked process as the second process (page 2, lines 22-30)]. Conventional kernels attempt to apply affinity-based scheduling to restart the pre-empted thread on any processing device core that accesses the same cache as the core that formerly executed that thread in the case of processing devices that are separate cores on a single die that share a common on-board cache.

Allowable Subject Matter

4. Claims 3-5, 7-19, 26-28, and 30-42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 20-23 43-46, and 48-49 are allowed.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vaswani et al. The Implications of Cache Affinity on Processor Scheduling for Multiprogrammed Shared Memory Multiprocessors ACM 1991.

Salehi et al., "The Effectiveness of Affinity-Based Scheduling in Multiprocessor Newtorking," 1996, pp. 215-233, IEEE.

US 7,107,593 (Jones et al) teaching predictable scheduling of programs using repeating precomputed schedules on discretely scheduled and/or multiprocessor operating systems.

US 6,289,369 (Sundaresan) teaching technique for dynamically exploiting affinity, locality, and load balancing in scheduling the execution of multi-threaded user programs in a multi-processor computer system utilizing central schedule queue.

US 6,269,391 (Gillespie) teaching scheduling kernel providing fair share scheduling of several virtual machines by a multi-processor scheduling module scheduling the virtual machines.

US 6,269,390 (Boland) teaching affinity scheduler affinitizing processes to processors so that processes which frequently modify the same data are affined to the same local processor--the processor whose cache memory includes the data being modified by the processes.

US 5,826,079 (Boland) teaching method for improving the execution efficiency of frequently communicating processes utilizing affinity process scheduling by identifying and assigning the frequently communicating processes to the same processor.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

September 28, 2006

PIERRE BATAILLE
PRIMARY EXAMINER